Method for Bonding Wafers to Produce Stacked Integrated Circuits

ABSTRACT

An integrated circuit wafer element and an improved method for bonding the same to produce a stacked integrated circuit. An integrated circuit wafer according to the present invention includes a substrate having first and second surfaces constructed from a wafer material, the first surface having a circuit layer that includes integrated circuit elements constructed thereon. A plurality of vias extend from the first surface through the circuit layer and terminate in the substrate at a first distance from the first surface. The vias include a stop layer located in the bottom of each via constructed from a stop material that is more resistant to chemical/mechanical polishing (CMP) than the wafer material. The vias may be filled with an electrically conducting material to provide vertical connections between the various circuit layers in a stacked integrated circuit. In this case, the electrical conducting vias are also connected to various circuit elements by metallic conductors disposed in a dielectric layer that covers the circuit layer. A plurality of bonding pads are provided on one surface of the integrated circuit wafer. These pads may be part of the vias. These pads preferably extend above the surface of the integrated circuit wafer. A stacked integrated circuit according to the present invention is constructed by bonding two integrated circuit wafers together utilizing the bonding pads. One of the integrated circuit wafers is then thinned to a predetermined thickness determined by the depth of the vias by chemical/mechanical polishing (CMP) of the surface of that integrated circuit wafer that is not bonded to the other integrated circuit wafer, the stop layer in the vias preventing the CMP from removing wafer material that is within the first distance from the first surface of the substrate of the wafer being thinned.